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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/594,510	06/16/2000	Alan G. Wood	M4065.0184/P184	2407

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EXAMINER	
LUU, CHUONG A	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 02/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/594,510	WOOD ET AL.	
	Examiner	Art Unit	
	Chuong A. Luu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23 and 35-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-23* is/are allowed.

6)☒ Claim(s) *1-18 and 35-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments, see the remark, filed December 23, 2004, with respect to the rejection(s)of claim(s) 1-18 and 35-38 under 102(e) rejection have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made of Yoon et al. (U.S. 6,479,887 B1) in view of Miyawaki (U.S. 6,268,236 B1).

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 1-18 and 35-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoon et al. (U.S. 6,479,887 B1) in view of Miyawaki (U.S. 6,268,236 B1).

Yoon discloses a semiconductor package with

Respect to claims:

(1) forming conductive structures (14, 23, 19, 13) in contact with a top surface of a dielectric substrate (18) (see Figure 2A);

subsequently, forming a layered assembly by attaching a wafer (2) to said dielectric substrate, such that said conductive traces are in electrical communication with semiconductor devices in said wafer (18) (see Figure 2B);

forming input/output devices (60) in contact with said conductive traces (14, 23, 19, 13) (see Figure 2E);

testing region (see column 11, lines 60-65);

subsequently, dicing said layered assembly (see column 13, lines 34-37. Figure 2F);

(2) further comprising the step of connecting said semiconductor devices to input/output devices (see column 13, lines 26-33. Figure 2E);

(3) wherein said testing is conducted through said input/output devices (see column 11, lines 60-65);

(4) further comprising the step of discarding one or more defective packages (see column 5, lines 20-25);

(5) wherein said step of forming said layered assembly includes the step of adhering said wafer to said dielectric substrate (see Figure 2B);

(6) further comprising the step of electrically connecting said semiconductor devices to ball grid arrays on said dielectric substrate (see Figure 2E);

(7) wherein said connecting step comprises the step of locating wire bonds in openings through said dielectric substrate (see Figures 2C-2D);

(8) wherein said connecting step comprises the step of connecting solder bumps on said wafer to circuit traces on said dielectric substrate (see Figure 2E);

(9); (17) wherein said dicing step is performed by a saw (see column 12, line 24-27);

(10) further comprising the step of providing an electrode pad in said layered assembly (see Figure 2A);

(11) providing conductive structures in contact with a top surface of a dielectric substrate (see Figure 1A);

subsequently, forming a layered assembly by attaching a wafer and a stiff metal layer to said dielectric substrate (see column 10, lines 50. Figure 1A);

placing ball grid arrays in contact with said conductive structures (see Figure 2E);

connecting semiconductor devices in said semiconductor wafer to said ball grid arrays (see column 13, lines 26-33. Figure 2E);

subsequently, dicing said layered assembly (see column 13, lines 34-37. Figure 2F);

(12) wherein said forming step comprises the step of adhering said wafer to said metal layer (see 2A-2B);

(13); (14) wherein said connecting step comprises the step of locating wire bonds in openings through said dielectric substrate (see Figures 2C-2D);

(15) wherein said connecting step comprises the step of connecting solder bumps on said wafer to conductive traces on said dielectric substrate (see Figures 2A-2E);

(16) further comprising the step of connecting said traces to conductive vias extending through said dielectric substrate (see Figure 2A).

(18) further comprising the step of testing said semiconductor devices through said ball grid arrays (see Figure 2E);

(35) adhering said wafer (2) to a flexible substrate (18) (see column 12, lines 7-40. Figures 2A-2B);

connecting said semiconductor devices to respective ball grid arrays (60) located on said substrate (see Figure 2E);

testing said semiconductor devices through said ball grid arrays (see column 11, lines 60-65);

(37) further comprising the step of singulating packages from said wafer and said substrate (see column 13, lines 26-37);

(36); (38) further comprising the step of segregating defective packages from other packages (see column 5, lines 20-25).

Yoon dicloses everything above except for further comprising the step of attaching said dielectric tape to said wafer by applying heat or pressure to the assembly; and further comprising the step of evacuating gas from said assembly. However, Miyawaki discloses a method of manufacturing a semiconductor chip by **(39)** further comprising the step of attaching said dielectric tape to said wafer by applying heat or pressure to the assembly (see column 4, lines 34-35); **(40)** further comprising the step of evacuating gas from said assembly (see column 5, lines 25-32). It would have been obvious to one having ordinary skill in the art at the time the invention was

made to modify the teaching of Yoon (in accordance with the teaching of Miyawaki) to attach the dielectric tape to said wafer by applying heat and pressure to the assembly; and further comprising the step of evacuating gas from said assembly during fabrication of a semiconductor device. Although, Yoon's reference is silent the step of testing semiconductor device; it would have been obvious that the testing should be taken place prior to further fabricating a semiconductor device. Doing so would facilitate the manufacture of the semiconductor device and reduce the time and cost by determining the deflective device prior to complete the semiconductor device.

Allowable Subject Matter

Claims 19-23 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong Anh Luu
Examiner
January 29, 2005